REMARKS

As a supplement to the Amendment filed July 21, 2003, the Applicants provide the following additional arguments in support of the patentability of claims 1-8 and 10-13.

Initially, the Applicants wish to sincerely thank Supervisor Utech for the courtesies extended to the Applicants' representatives during the personal interview of July 21, 2003.

The Applicants repeat the arguments of the July 21st Amendment in support of the patentability of claim 1-8 and 10-13 over the rejections of:

> Claims 1-16, under 35 U.S.C. § 103(a), as being obvious in view of the teachings of Tung ('625) combined with the teachings of Sugano et al et al ('527),
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> Claims 1-16, under 35 U.S.C. § 103(a), as being obvious in view of the teachings of Maa et al ('775) combined with the teachings of Sugano et al et al ('527), and
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> Claims 9 and 14-16, rejected under 35 U.S.C. § 103(a), as being obvious in view of the teachings of Tung ('625) or Maa et al ('775) combined with the teachings of Sugano et al et al ('527) and Yamazaki et al ('579),

and to those arguments add the following.

As noted previously the presently claimed invention is directed generally to a process for fabricating a semiconductor device including the steps of:

> distributing a nonmetal element composed of an oxygen element, a nitrogen element or a flouring element in a region in the vicinity of a surface portion of a semiconductor layer, and thereafter,
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> depositing a metal film on the semiconductor layer, and
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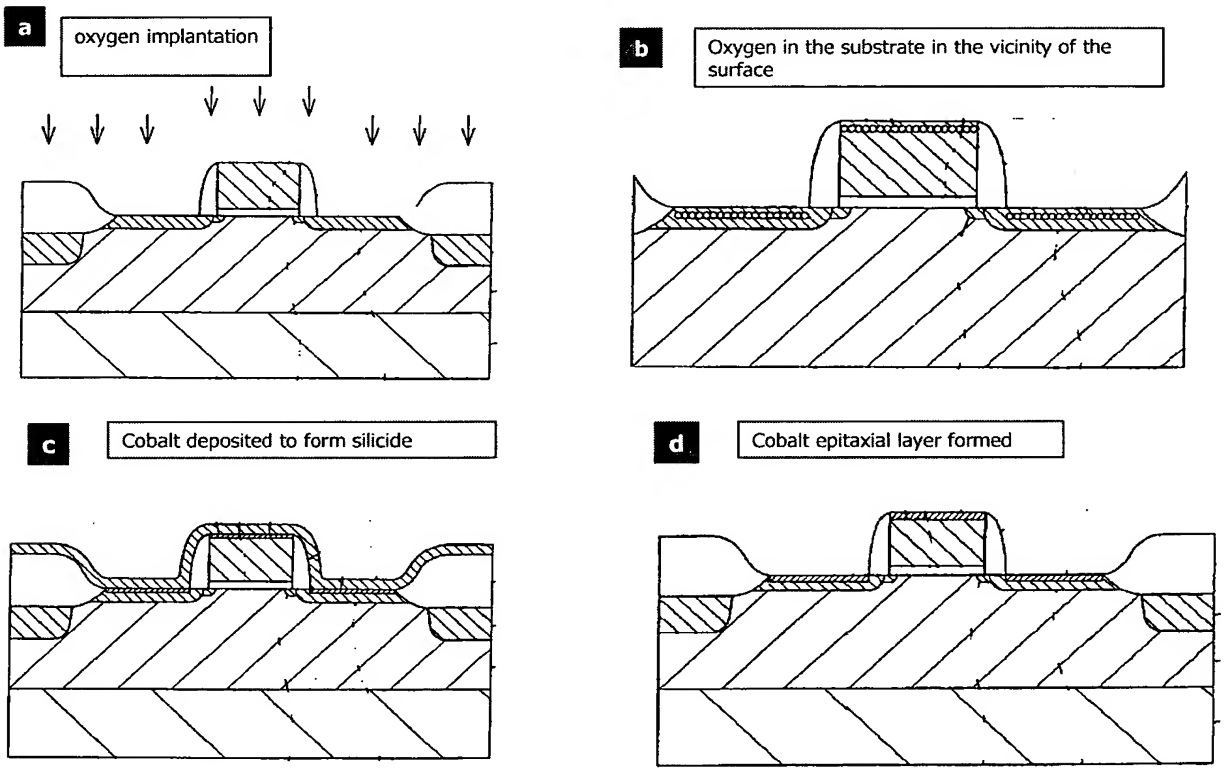
> epitaxially growing a semiconductor-metal compound layer in the surface portion of said semiconductor layer by causing a reaction between the element included in the semiconductor layer and a metal included in the metal film by annealing of the metal film.

Further, as discussed previously, since the nonmetal element composed of an oxygen element, a nitrogen element or a fluorine element is distributed in a region in the vicinity of the surface portion of the semiconductor layer and since the oxygen, nitrogen and fluorine elements are different from the elements, such as arsenic,

phosphorus, boron and indium, used in the manufacture of the diffusion layers or regions in a semiconductor device, there will be no adverse effect upon the diffusion layers upon employing the oxygen, nitrogen or fluorine elements as claimed.

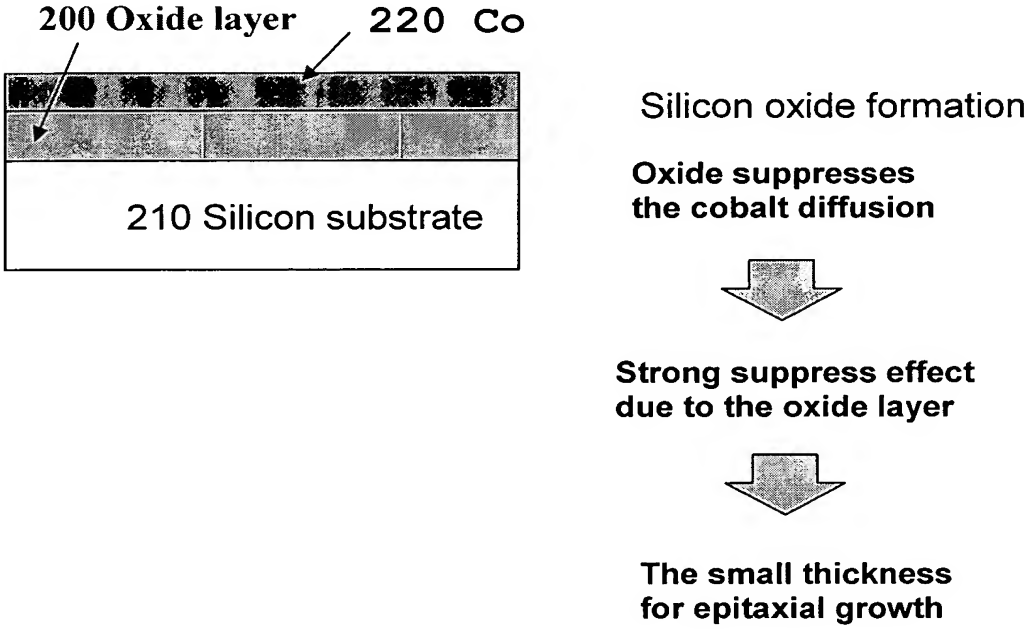
In one embodiment of the invention, illustrated below and in Figures 3(a)-3(c) as well as in claim 11, oxygen atoms are distributed in the surface of the (N-type) high concentration impurity layer (108) or the surface of the gate electrode (105) by O_2 implantation via plasma doping to be followed later by epitaxial Co layer being grown:



Accordingly, subsequent diffusion of the deposited (cobalt) metal atoms into either the high concentration impurity layer (108) or the gate electrode (105) above is prevented due to this distribution of the oxygen atoms in this vicinity of the surface portion of the high concentration impurity layer (108), or the gate electrode (105). That is, as discussed in the specification at page 20, line 3, to page 21, line 2, rapid reaction of the (cobalt) metal atoms and the (silicon) semiconductor atoms can be

prevented which avoids the agglomeration and polycrystallization, discussed in the background of the specification at page 3, due to pinholes in the surface oxide. Consequently, a thick (cobalt silicide) semiconductor-metal compound can be formed by epitaxial growth.

The Examiner's discussion of the Tung reference, as illustrated below and in Figure 2B below, notes the formation of a thin oxide layer (200) having a thickness of 0.5 to about 1.5 nm on the surface of a silicon substrate (210).



As noted in the July 21st amendment, this oxide layer (200) is formed by subjecting the surface of the substrate to a chemical cleaning solution (column 5, lines 33-39), and the cobalt layer (220) is formed over the oxide layer (200). The uniform thickness cobalt layer (220) is formed by e-beam evaporation or sputter deposition (column 5, lines 62-66). The cobalt layer (220) is then annealed for an amount of time sufficient to convert the cobalt to cobalt silicide (column 6, lines 11-19).

Applicants again assert that such a teaching in Tung does not teach the step of distributing the (oxygen, nitrogen, fluorine) nonmetal element (109) in the region in the vicinity of the surface portion of the semiconductor layer (110) as explicitly set forth in each embodiment of the invention in the specification, i.e., Figures 3(a)-3(c),

6(a)-6(c) and page 17, line 5, to page 18, line 8, and page 27, line 1, to page 28, line 4. Clearly, Tung does not distribute the (oxygen, nitrogen, fluorine) nonmetal element (109) inside the surface of the semiconductor as presently claimed, but instead forms an oxide on the surface of the substrate.

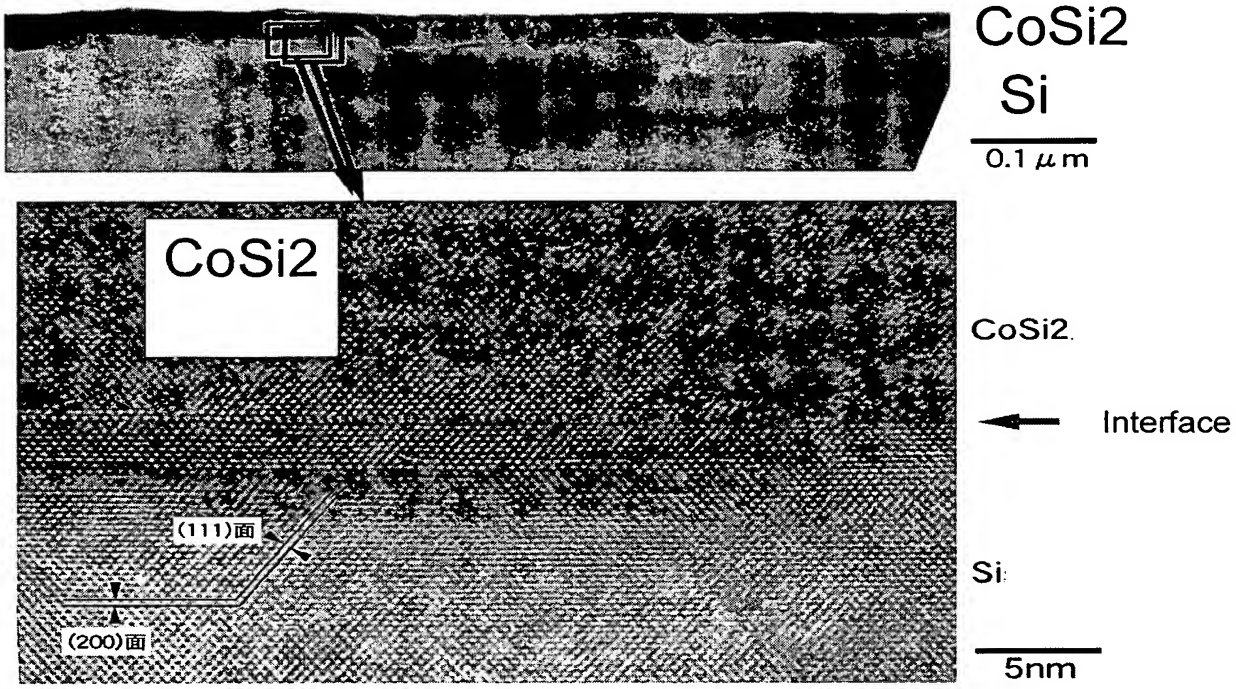
Applicants take particular note of the teaching in the specification, at page 27, lines 6-25, that the mere application of a silicon oxide on the surface of the semiconductor does not result in the distribution of the (oxygen, nitrogen, fluorine) nonmetal element (109) inside the surface of the semiconductor as presently claimed, but instead the claimed distribution occurs when the silicon oxide coated surface is irradiated with a (Ar) particle beam.

To remedy this acknowledged deficiency, the Examiner relies upon the teachings of the Sugano et al reference. However, Sugano et al teach depositing (see Figure 15B) on the silicon substrate (32) a silicon oxide (SiO_2) film (31) which is then irradiated with a neutron beam to produce lattice defects throughout the irradiated region of the silicon substrate (32) so as to make the silicon substrate semi-insulating (see Figure 15B). Thereafter, the silicon substrate (32) is annealed by irradiating the substrate (32) with laser beam pulses to form an activated layer (33) in the surface portions of the substrate (32) adjacent the silicon oxide film (31). The silicon oxide film is then removed and two ohmic contacts (34) are formed on the activated layer (33) (see column 11, line 67, to column 12, line 11).

However, Sugano et al fail to explicitly teach the step of distributing oxygen in the region in the vicinity of the surface portion of the semiconductor for any reason. The Examiner attempts to overcome this acknowledged deficiency of Sugano et al by stating that such a formation is inherent since a "similar irradiation of the compound layer with a particle beam" takes place in Sugano et al as in the presently disclosed invention. The method of Sugano et al does appear to be similar to that taught by specification at Embodiment 3 and Figures 6(a)-6(c). However, there are several important differences.

The first is that a neutron beam irradiation apparatus, not an Ar ion beam irradiation apparatus, is used employed and the second difference is that the irradiation is carried out to produce lattice defects in the substrate. That is, as one of ordinary skill in the prior art is well aware, a neutron beam apparatus employs neutron particles and operates at a much higher energy level than an ion implantation apparatus. This high energy level is necessary for the method of Sugano et al since lattice defects (faults/fractures) must be produced in the substrate which requires considerably higher energy (electron volt) particle beams than an ion beam apparatus. See the U.S. Patent Nos. 4,992,298 and 4,861,750 (regarding keV ranges for Ar+ ion beam devices for semiconductors) and the Moll et al article entitled "Relation Between Microscopic Defects And...After Hadron Irradiation" and the Gersey et al article entitled "Neutron Dosimetry Using...Silicon Equivalent Proportional Counters For Eight High-Energy Neutron Spectra" (regarding conventional neutron apparatus for treating semiconductor devices) for teachings of this well known difference.

Additionally, as the Examiner is also well aware, it is well known that the formation of lattice defects in a conventional semiconductor substrate (i.e., crystalline substrate) will greatly inhibit the growth of any epitaxial layer thereon since each defect will serve as a nucleating site for another crystal resulting in polycrystalline growth instead of the epitaxial growth of the claimed invention. The epitaxial growth of the claimed invention is shown in the photomicrograph below. Note, the same crystal orientation continues from the substrate into the epitaxial $CoSi_2$ layer:



Therefore, even if combined with the teachings of Tung, the resulting process would form lattice defects in the substrate of Tung which would prevent formation of an epitaxial layer of $CoSi_2$ of the presently claimed invention.

The Applicants continue to assert that the Examiner's inherency position with regard to Sugano et al is technically incorrect (for the reasons set forth above) and inconsistent with U.S. law and USPTO practice regarding the establishment of a proper case of inherency. That is, MPEP Chapter 2112 sets forth the requirements for the Examiner in establishing "inherency" (see July 21st Amendment) and based upon those requirements and a review of the teachings of Sugano et al above, it is clear that one of ordinary skill in the prior art would not readily recognize that the neutron beam irradiation process of Sugano et al (which is not the same as the instantly disclosed Ar ion beam doping irradiation process) of a silicon oxide layer would result in oxygen atoms from the oxide layer being distributed in the vicinity of the semiconductor as presently disclosed and claimed. Specifically, one of ordinary skill in the prior art would realize that the neutron beam of Sugano would readily form lattice defects in

the semiconductor substrate. Further, it is also noted that Sugano is silent as to the constituents of the silicon oxide layer (31) being present inside the surface (in the vicinity) of the semiconductor layer (32).

As discussed previously, Maa et al (see Figure 2) teach that an active area (32) is formed on an oxide layer (14) on a substrate (10). The source (46) and drain (48) regions are formed (see column 3, lines 52-65) after providing the gate structure (30). Next, Maa et al (see Figure 4) teach depositing a layer of silicidation (cobalt) material (80) on the substrate (see column 4, line 55, to column 5, line 4). Then a RTA process is performed (see Figure 5) to form a silicide at the boundary between the silicidation (cobalt) material (80) and the source (46) and drain (48) regions (see column 5, lines 5-15).

Note, the patentees (see column 6, lines 50-63) teach that any *in situ* surface oxide formed on the surface of the silicide must be removed, such as by use of an Ar ion beam. This last step (of Ar beam cleaning of a surface oxide on a silicide) of Maa et al is not in any manner similar to the distribution of (oxygen) a nonmetal element (109) in the region in the vicinity of the surface portion of the semiconductor layer (110) via Ar ion beam irradiation of a silicon oxide layer as set forth in the specification, i.e., Figures 6(a)-6(c) and page 27, line 1, to page 28, line 4.

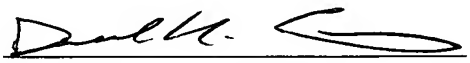
Therefore, it can also be seen that the Maa et al reference does not teach the step of distributing the (oxygen, nitrogen, fluorine) nonmetal element (109) in the region in the vicinity of the surface portion of the semiconductor layer (110) as explicitly set forth (defined) in each embodiment of the invention in the specification, i.e., Figures 3(a)-3(c), 6(a)-6(c) and page 17, line 5, to page 18, line 8, and page 27, line 1, to page 28, line 4. That is, Maa et al do not distribute the (oxygen, nitrogen, fluorine) nonmetal element (109) inside the surface of the semiconductor as presently claimed. To remedy this deficiency, the Examiner again relies upon the teachings of the Sugano et al reference. However, Sugano et al, for the reasons discussed above, does not explicitly or implicitly (inherently) teach distributing the (oxygen, nitrogen, fluorine) nonmetal element (109) in the region in the vicinity of the surface portion of

the semiconductor layer (110) as presently claimed. Again, as discussed above, upon combining the teachings of Sugano et al with those of Maa et al, the resulting process would form lattice defects in the substrate which would mitigate against the subsequent formation of an epitaxial $CoSi_2$ layer on the substrate.

Finally, since Sugano et al, Maa et al and Tung are deficient for the reasons as discussed above, the references cannot be combined with proper motivation to (explicitly or inherently) teach or suggest the presently claimed invention and further, even if combined, would not yield a process as presently claimed since the surface of the semiconductor substrate would contain lattice defects detrimental to epitaxial growth. Consequently, the rejections of claims 1-16, under §103(a), have been set forth in error and must be withdrawn.

Having responded to the rejection set forth in the outstanding Final Office Action, it is submitted that claims 1-8, 10-13 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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